IN THE CLAIMS

Please amend the claims as follows:

1. (Withdrawn) A method comprising:

receiving a first frame, wherein the first frame includes an overhead portion and data portion;

converting the first frame into a second frame, wherein the second frame comprises a programmable size and wherein the second frame includes column and row parity information and the overhead portion and the data portion;

specifying locations of column and row parity information within the second frame, wherein a synchronization information represents the column and row parity information locations; and

converting the second frame into a third frame, wherein the third frame includes the overhead portion, the data portion, the column and row parity information, and the synchronization information.

2. (Withdrawn) The method of Claim 1, wherein a percentage of the overhead portion and the data portion within the second frame is equal to the percentage of the overhead portion and the data portion within the first frame.

3. (Withdrawn) The method of Claim 1, wherein the second frame comprises a configurable length and width.

4. (Withdrawn) The method of Claim 1, wherein the column and row parity information locations within the second frame are programmable.

5. (Withdrawn) The method of Claim 1, wherein the converting the first frame into the second frame comprises:

reserving column and row parity locations within the second frame; and

inserting the column and row parity information within the reserved locations.

6. (Withdrawn) The method of Claim 1, wherein the converting the first frame into the second frame comprises performing Bose, Chaudhuri and Hocquenghem encoding to provide the column and row parity information.

7. (Withdrawn) The method of Claim 1, wherein the converting the first frame into the second frame comprises performing Reed Solomon encoding to provide the column and row parity information.

8. (Withdrawn) The method of Claim 1, wherein the third frame comprises an error correction portion and further comprising storing the synchronization information within the error correction portion.

9. (Withdrawn) The method of Claim 1, wherein the third frame is the same size as that of the first frame.

10. (Withdrawn) The method of Claim 1, wherein the programmable size is based on a level of forward error correction encoding.

11. (Withdrawn) The method of Claim 1, further comprising specifying locations of the synchronization information within the third frame.

12. (Withdrawn) The method of Claim 1, wherein a concatenation style of the second frame is either stream or block oriented.

13. (Withdrawn) A method comprising:

receiving a first frame, wherein the first frame includes an overhead portion, data portion, and a synchronization information;

converting the first frame into a second frame, wherein the second frame comprises a programmable size and includes column and row parity information and further includes the overhead portion and the data portion;

performing forward error correction on the second frame; and

converting the second frame into a third frame, wherein the third frame includes the overhead portion and the data portion.

14. (Withdrawn) The method of Claim 13, wherein the converting the first frame into the second frame further comprises:

determining locations of column and row parity information within the second frame based on the synchronization information; and

providing the column and row parity information within the determined locations.

15. (Withdrawn) The method of Claim 13, wherein the performing forward error correction comprises performing iterative forward error correction.

16. (Withdrawn) The method of Claim 13, wherein the performing forward error correction comprises performing concatenated forward error correction.

17. (Withdrawn) The method of Claim 13, wherein the performing forward error correction comprises performing Bose, Chaudhuri and Hocquenghem processing.

18. (Withdrawn) The method of Claim 13, wherein the performing forward error correction comprises performing Reed Solomon processing.

19. (Withdrawn) The method of Claim 13, wherein the third frame further includes an error correction portion and further comprising storing the synchronization information within the error correction portion.

20. (Withdrawn) The method of Claim 19, wherein the error correction portion includes column and row parity information.

21. (Withdrawn) The method of Claim 13, wherein the third frame is the same size as that of the first frame.

22. (Original) An apparatus comprising:

a first mapper to convert a first frame into a second frame, wherein the first frame includes an overhead portion and data portion and wherein the second frame comprises a programmable size and wherein the second frame includes column and row parity information and the overhead portion and the data portion;

a synchronizer to specify locations of column and row parity information within the second frame, wherein a synchronization information represents the column and row parity information locations;

an encoder to insert column and row parity information into the second frame; and

a second mapper to convert the second frame into a third frame, wherein the third frame includes the overhead portion, the data portion, the column and row parity information, and the synchronization information.

23. (Original) The apparatus of Claim 22, wherein a percentage of the overhead portion and the data portion within the second frame is equal to the percentage of the overhead portion and the data portion within the first frame.

24. (Original) The apparatus of Claim 22, wherein the second frame comprises a configurable length and width.

25. (Original) The apparatus of Claim 22, wherein the column and row parity information locations within the second frame are programmable.

26. (Original) The apparatus of Claim 22, wherein the first mapper to convert the first frame into the second frame is to perform Bose, Chaudhuri and Hocquenghem encoding to determine the column and row parity information.

27. (Original) The apparatus of Claim 22, wherein the first mapper to convert the first frame into the second frame is to perform Reed Solomon encoding to determine the column and row parity information.

28. (Original) The apparatus of Claim 22, wherein the third frame comprises an error correction portion to store the synchronization information.

29. (Original) The apparatus of Claim 22, wherein the third frame is the same size as that of the first frame.

30. (Previously Presented) The apparatus of Claim 22, wherein the programmable size is based on a level of forward error correction encoding.

31. (Original) The apparatus of Claim 22, wherein the second mapper is to specify locations of the synchronization information within the third frame.

32. (Original) The apparatus of Claim 22, wherein a concatenation style of the second frame is either stream or block oriented.

33. (Original) An apparatus comprising:

a synchronizer to determine locations of column and row parity information within a first frame;

a first mapper to convert the first frame into a second frame, wherein the first frame includes an overhead portion, data portion, and a synchronization information and wherein the second frame comprises a programmable size and includes column and row parity information and further includes the overhead portion and the data portion;

a decoder to perform forward error correction on the second frame; and

a second mapper to convert the second frame into a third frame, wherein the third frame includes the overhead portion and the data portion.

34. (Original) The apparatus of Claim 33, wherein the first mapper is to store column and row parity information within the second frame based on the synchronization information.

35. (Original) The apparatus of Claim 33, wherein the decoder to perform forward error correction is to perform iterative forward error correction.

36. (Original) The apparatus of Claim 33, wherein the decoder to perform forward error correction is to perform concatenated forward error correction.

37. (Original) The apparatus of Claim 33, wherein the decoder to perform forward error correction is to perform Bose, Chaudhuri and Hocquenghem processing.

38. (Original) The apparatus of Claim 33, wherein the decoder to perform forward error correction is to perform Reed Solomon processing.

39. (Original) The apparatus of Claim 33, wherein the third frame further includes an error correction portion to store the synchronization information.

40. (Original) The apparatus of Claim 39, wherein the error correction portion includes column and row parity information.

41. (Original) The apparatus of Claim 33, wherein the third frame is the same size as that of the first frame.

42. (Original) A system comprising:

a data processor comprising:

a first mapper to convert a first frame into a second frame, wherein the first frame includes an overhead portion and data portion and wherein the second frame comprises a programmable size and wherein the second frame includes column and row parity information and the overhead portion and the data portion,

a synchronizer to specify locations of column and row parity information within the second frame, wherein a synchronization information represents the column and row parity information locations,

an encoder to insert column and row parity information into the second frame, and

a second mapper to convert the second frame into a third frame, wherein the third frame includes the overhead portion, the data portion, the column and row parity information, and the synchronization information; and

an interface to provide and receive signals from the data processor.

43. (Original) The system of Claim 42, wherein the interface is compatible with XAUI.

44. (Original) The system of Claim 42, wherein the interface is compatible with IEEE 1394.

45. (Original) The system of Claim 42, wherein the interface is compatible with PCI.

46. (Original) The system of Claim 42, further comprising a switch fabric coupled to the interface.

47. (Original) The system of Claim 42, further comprising a packet processor coupled to the interface.

48. (Original) The system of Claim 42, further comprising a bus to exchange signals with the data processor.

49. (Original) The system of Claim 48, further comprising a memory device coupled to the bus.

50. (Original) The system of Claim 42, wherein the data processor is to perform media access control in compliance with IEEE 802.3.

51. (Previously Presented) The system of Claim 42, wherein the data processor is to perform optical transport network framing in compliance with ITU-T G.709.

52. (Previously Presented) The system of Claim 42, wherein the data processor is to perform forward error correction encoding in compliance with ITU-T G.975.

53. (Original) A system comprising:

a data processor comprising:

a synchronizer to determine locations of column and row parity information within a first frame,

a first mapper to convert the first frame into a second frame, wherein the first frame includes an overhead portion, data portion, and a synchronization information and wherein the second frame comprises a programmable size and includes column and row parity information and further includes the overhead portion and the data portion,

a decoder to perform forward error correction on the second frame, and

a second mapper to convert the second frame into a third frame, wherein the third frame includes the overhead portion and the data portion; and

an interface to provide and receive signals from the data processor.

54. (Original) The system of Claim 53, wherein the interface is compatible with XAUI.

55. (Original) The system of Claim 53, wherein the interface is compatible with IEEE 1394.

56. (Original) The system of Claim 53, wherein the interface is compatible with PCI.

57. (Original) The system of Claim 53, further comprising a switch fabric coupled to the interface.

58. (Original) The system of Claim 53, further comprising a packet processor coupled to the interface.

59. (Original) The system of Claim 53, further comprising a bus to exchange signals with the data processor.

60. (Original) The system of Claim 59, further comprising a memory device coupled to the bus.

61. (Original) The system of Claim 53, wherein the data processor is to perform media access control in compliance with IEEE 802.3.

62. (Original) The system of Claim 53, wherein the data processor is to perform optical transport network de-framing in compliance with ITU-T G.709.

63. (Original) The system of Claim 53, wherein the data processor is to perform forward error correction processing in compliance with ITU-T G.975.